M88MR5RCD01

Gen1 DDR5 MRCD for MRDIMM / MCRDIMM

General Description

The M88MR5RCD01 is a first-generation DDR5 Multiplexed Rank Registering Clock Driver (MRCD) chip that supports data rates of up to 8800MT/s. This chip buffers and re-drives the address, command, clock, and control signals from the memory controller. Compared to traditional DDR5 RCD chips, the MRCD can generate four independent chip-select signals at standard rates, enabling more flexible and efficient memory management operations. Working in conjunction with Multiplexed Rank Data Buffer (MDB) chips, the MRCD chip is applied in next-generation DDR5 MRDIMM / MCRDIMM memory modules, effectively doubling memory system bandwidth to meet the urgent demand for memory throughput in high-performance computing scenarios, such as AI training, inference, and large-scale data analysis.

Application

- DDR5 MRDIMM / MCRDIMM

Feature

- Speed up to 8800MT/s
- Two sub-channels, each divided into two pseudo-channels to increase the total bandwidth of the host system
- Two pseudo-channels splitting the incoming CA inputs and generating separate CA outputs
- Integrated PLL clock driver distributing one differential clock pair to five differential pairs per channel
- Parity checking across CA and DPAR inputs separately on two sub-channels
- Integrated BCOM bus to control the multiplexed data buffers (MDB)
- Output characteristics configurable through control word registers
- Sideband bus interface supporting I²C and I3C Basic modes
- CA, CS, DFE and BCOM training modes support
- Multiple power-saving modes
- 1.1V VDD and 1.0V VDDIO voltages
- Green package: 240-ball FBGA

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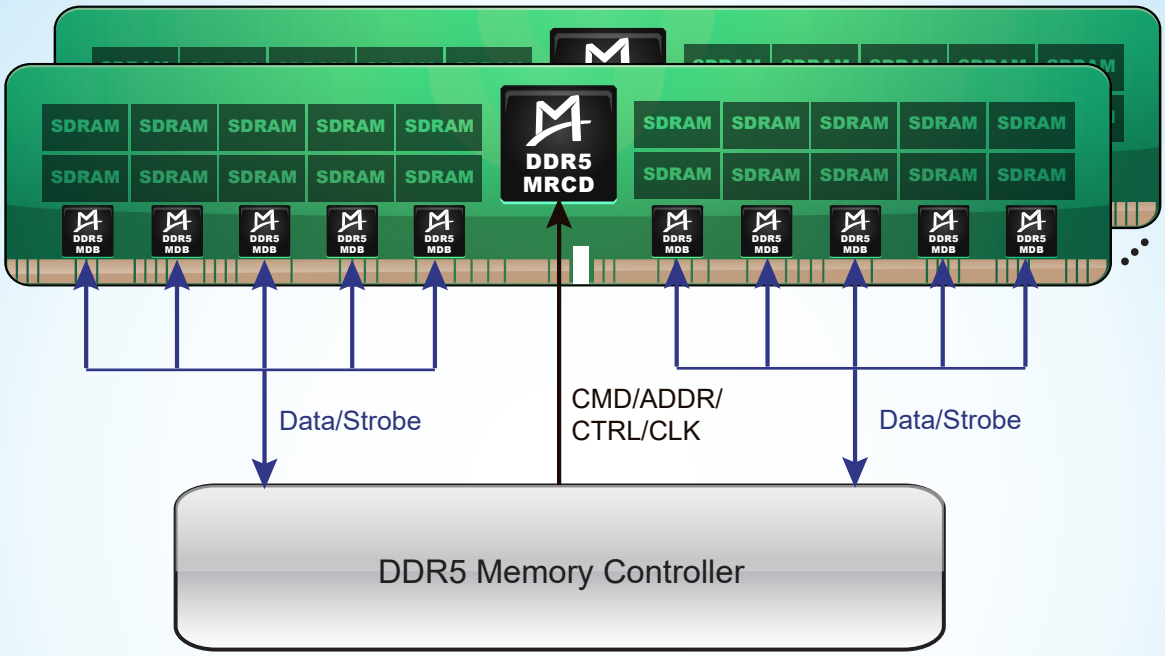
Application Diagram



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