M88MR5DB01

Gen1 DDR5 MDB for MRDIMM / MCRDIMM

General Description

The M88MR5DB01 is a Gen1 DDR5 Multiplexed Data Buffer (MDB) supporting data rates up to 8800MT/s. The MDB chip buffers and re-drives data signals from the memory controller or DRAM devices. It incorporates a dual-nibble host interface that operates at twice the speed of the DRAM interface. The DRAM side features four nibbles, with two allocated to each pseudo-channel. The MDB efficiently multiplexes two DRAM-side DQ signals into one host-side DQ signal.

Designed to work in conjunction with the Multiplexed Registering Clock Driver (MRCD), the MDB plays a crucial role in DDR5 MRDIMMs / MCRDIMMs. Each MRDIMM / MCRDIMM is equipped with one MRCD and ten MDBs. This configuration enables the MRDIMM / MCRDIMM module to concurrently access two DRAM memory ranks through the MDB chips, resulting in a doubling of bandwidth to address the demands of high-load applications.

Applications

- DDR5 MRDIMM / MCRDIMM

Feature

- Speed up to 8800MT/s
- Dual nibbles on the host side
- Four nibbles on the DRAM side, two per pseudo-channel
- Two DRAM-side DQ signals multiplexed to one host-side DQ signal
- One input-only control bus interface for connecting to a Multiplexed Rank Registering Clock Driver (MRCD)
- x4 and x8 DRAMs support
- Strobe and data training support
- DRAM periodic update support
- Multiple power-saving modes
- Transparent, continuous burst, loopback and pass-through modes support
- 1.1V VDD voltage
- Green package: 78-Ball FBGA

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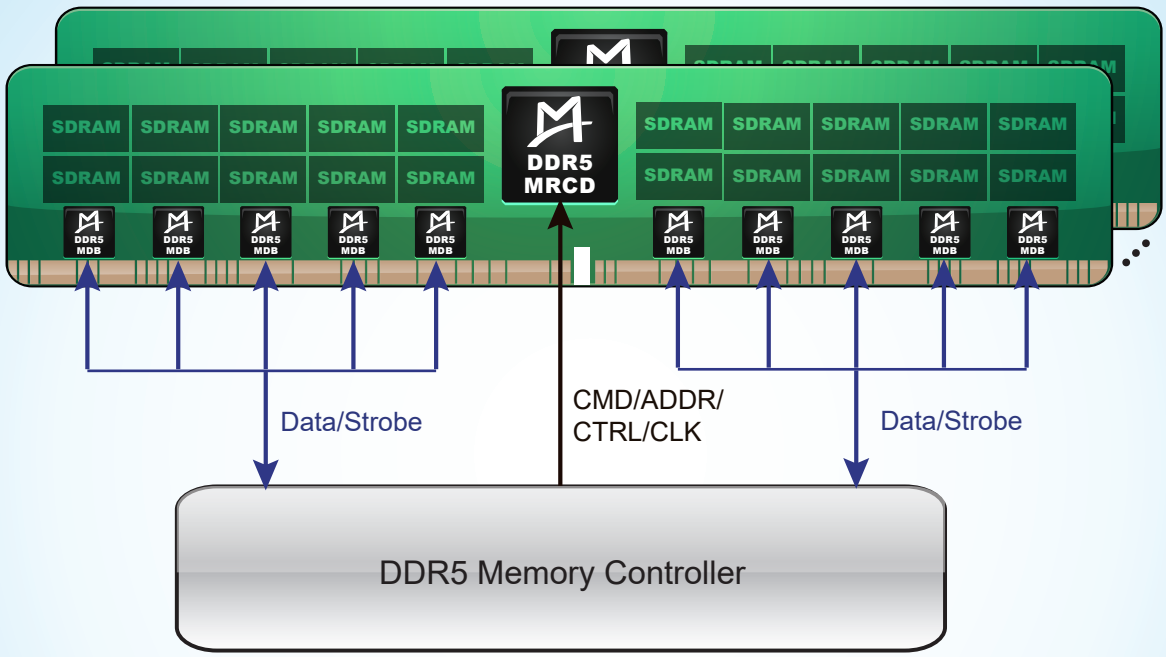
Application Diagram



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